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Inventor(s): Re:

MING XI, PAUL FREDERICK SMITH, LING CHEN, MICHAEL X. YANG, MEI

CHANG, FUSEN CHEN, CHRISTOPHE MARCADAL and JENNY C. LIN

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

Transmitted herewith is the patent application identified above, including:

- X Specification, claims and abstract, totaling 21 pages.
- X Drawings totaling 5 pages, X Formal Informal.
- <u>X</u> Executed Declaration and Power of Attorney.
- Information Disclosure Statement w/ Form 1449 and References.
- X Assignment of the invention to Applied Materials, Inc.

X Assignment Recordation Cover Sheet

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FEE CALCULATION							
Fee Items	Claims Filed	Included With Basic Fee	Extra Claims	Fee Rate	Total		
Total Claims	40	-20=	20	x \$18.00	\$360.00		
Independent Claims	7	-3=	4	x \$84.00	\$336.00		
Basic Filing Fee \$ 740.00							
TOTAL FEES	\$1,436.00						

- X The Commissioner is hereby authorized to charge \$1,436.00 to Deposit Account No. 50-1074/1931.P1/CPI/ALUMINUM/PJS/RWM.
- X The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1074/1931.P1/CP/ALUMINUM/PJS/RWM. A duplicate copy of this transmittal is enclosed.
- <u>X</u> Please address all future correspondence to:

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Respectfully submitted

ROBERT W. MULCAHY

Registration No. 25,436

UNITED STATES PATENT APPLICATION FOR:

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

INVENTORS:

MING XI **PAUL FREDERICK SMITH** LING CHEN MICHAEL X. YANG **MEI CHANG FUSEN CHEN** CHRISTOPHE MARCADAL JENNY C. LIN

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CERTIFICATION OF MAILING UNDER 37 C.F.R. 1.10

I hereby certify that this New Application and the documents referred to as enclosed therein are being Dich deposited with the United States Postal Service on Signature 1-17-02, in an envelope marked as "Express Mail United States Postal Service", Mailing Label No. EV041916406US, addressed to: Assistant Name Commissioner for Patents, Box PATENT APPLICATION, Washington, D.C. 20231.

Date of signature

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

Related Applications

This application is a continuation-in-part of pending United States Patent [0001]

Application No. 08/856,116, filed May 14, 1997, and which is hereby incorporated by

reference.

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BACKGROUND OF THE INVENTION

Field of the Invention

[0002] Embodiments of the invention relate to a deposition sequence and related

hardware for manufacturing a plug and line typical of a dual damascene structure

utilizing a thin conformal barrier layer formed on the walls of the feature.

Description of the Related Art

[0003] Modern semiconductor integrated circuits usually involve multiple

conductive layers separated by dielectric (insulating) layers, such as oxide layers.

The conductive layers are electrically interconnected by holes penetrating the

intervening oxide layers and contacting some underlying conductive feature. After

the holes are etched, they are filled with a metal, typically aluminum or copper, to

electrically connect the conductive layers with each other. In a circuit formed by a

dual damascene process, there are two types of holes, vias and trenches, which

penetrate dielectric layers of the circuit. Vias are holes which extend to an

underlying conductive feature. Vias which are filled with a metal are called plugs, or

via plugs. Trenches are holes which extend into the dielectric layer of the circuit, but

do not extend to an underlying conductive feature. Trenches which are filled with a

metal are called lines, which serve as horizontal interconnects in a circuit.

As sizes of features such as holes in integrated circuits continue to [0004]

decrease, the characteristics of the material forming the plugs become increasingly

important. The smaller the plug, the less resistive the material forming the plug

should be for speed performance. Copper is a material which is becoming more

important as a result. Copper has a resistivity of 1.7 $\mu\Omega$ -cm. Copper has a small

RC time constant thereby increasing the speed of a device formed thereof. In

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addition, copper exhibits improved reliability over aluminum in that copper has excellent electromigration resistance and can drive more current in the lines.

One problem with the use of copper is that copper diffuses into silicon [0005] dioxide, silicon and other dielectric materials. Therefore, barrier layers become increasingly important to prevent copper from diffusing into the dielectric materials and compromising the integrity of the device. Barrier materials such as Ta, TaN, SiN, Ti, TiN, W, and WN on the interlayer dielectric will effectively inhibit interlayer diffusion. However, within the same dielectric layer it is difficult to provide an effective barrier to prevent leakage between lines. Several technologies, such as physical vapor deposition (PVD), are presently under investigation for adding a barrier layer to the via sidewall separating the copper metal from the interlayer dielectric. However, common PVD technologies are limited in high aspect structures due to the directional nature of their deposition. Thus, the thickness of a barrier layer deposited by PVD will depend directly upon the structure architecture, with the barrier becoming thinner on the sidewall near the structure bottom. The barrier thickness, and therefore the barrier integrity may be compromised on the sidewall near the structure bottom. Also, the bottom corners of vias often do not form precise right angles at their intersection. Instead, there may be recesses or "undercuts" 11 at the bottom corners of vias 10 formed in a dielectric layer 12, as shown in Fig. 1. As a result, it is difficult to deposit a barrier layer that covers these undercuts by PVD because of the limited directionality of deposition by PVD.

[0006] In contrast, chemical vapor deposition (CVD) and atomic layer deposition (ALD) deposited films are, by their nature, conformal in re-entrant structures. Silicon nitride (Si_xN_y) and titanium nitride (TiN) prepared by decomposition of an organic material, tetrakis(dimethylamido) titantium (TDMAT) are common semiconductor manufacturing materials which display the described conformal performance. Both materials are perceived as being good barriers to Cu diffusion, but are considered unattractive due to their high resistivity. The highly resistive nature of these materials detrimentally affects the conductivity between the plug and the underlying conductive features, which must be maintained as low as possible to maximize logic device performance.

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[0007] Therefore, there is a need for a process sequence and related hardware which provides a good barrier layer on the via sidewall, but which does not negatively affect the conductivity of the plug.

SUMMARY OF THE INVENTION

[0008] Embodiments of the present invention generally provide a process and related hardware for filling a patterned feature on a substrate with copper or other conductive materials. One embodiment of the present invention comprises forming a generally conformal CVD or ALD barrier layer over a patterned feature formed in a substrate, etching the barrier layer at the bottom of the patterned feature, depositing a second barrier layer that does not significantly impact conductivity between the plug and the underlying layer, but provides an adequate barrier on other surfaces, and then filling the patterned feature with a conductive material, such as copper. Another embodiment of the present invention comprises forming a generally conformal CVD or ALD barrier layer over a patterned feature formed in a substrate having an etch stop, etching the barrier layer and the etch stop at the bottom of the patterned feature, depositing a second barrier layer, and then filling the patterned feature with a conductive material, such as copper.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the features of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0010] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0011] Figure 1 is a partial cross-sectional view of a substrate having undercuts at the bottom of its via, as known in the prior art;

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[0012] Figures 2-8 are partial cross-sectional views of a substrate having one process sequence of the present invention performed thereon;

[0013] Figure 9 is a schematic of a multichamber processing apparatus;

[0014] Figure 10 is a cross-sectional view of a CVD process chamber; and

[0015] Figure 11 is a cross-sectional view of a PVD process chamber.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] Figures 2-8 illustrate and describe one embodiment of a process sequence of the present invention. Figure 2 is a partial cross sectional view of a substrate having a via 200 and a trench 202 formed thereon through a dielectric layer 204 to an underlying metal layer 206. A conformal barrier layer 208, shown in Figure 3, is formed over the patterned surface by CVD techniques, such as conventional CVD and rapid CVD, or atomic layer deposition (ALD). The barrier layer deposited by CVD may be formed from materials such as Si_xN_y, TiSi_xN, TiN(C), TiNSi(C), Ta, TaC, TaN(C), TaNSi(C), W, WN_x, SiO_xN_y, SiC, AlN, or Al₂O₃.

[0017] While the barrier layer 208 deposited by CVD or ALD provides desired conformal coverage of a substrate, including the sidewalls 216 and 218 of the via and the trench, respectively (Figure 4), the barrier layer 208 also covers the lower portion of the via (Figure 3), which contacts the underlying metal layer 206. The barrier layer 208 on the underlying metal layer 206 increases the resistance of the overall structure, and negatively impacts the performance of the structure. Thus, the substrate is exposed to a pre-clean or other etching process, such as an argon/hydrogen etch process to remove a portion of the barrier layer formed on the horizontal surfaces of the patterned feature, i.e, the bottom of the via 210 at the interface with the underlying metal layer 206, the bottom of the trench 212, and the field surface 214, as shown in Figure 4. The etching may also extend into and remove part of the underlying metal layer (not shown). Preferably, the etching process is performed within a system that also includes the chamber in which the barrier layer 208 is deposited by chemical vapor deposition, so that the substrate is not exposed to air. More preferably, the etching process is performed within the

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same chamber in which chemical vapor deposition of the barrier layer is performed. However, in another embodiment, there is an air break in which the substrate is moved out of the processing system after the deposition of the barrier layer 208 and before the etching process.

[0018] Removing the barrier layer 208 from the bottom of the via 210 ensures a good, low resistance electrical contact to the underlying metal layer 206. However, removing the barrier layer 208 from another surface of the patterned feature, i.e., the bottom of the trench 212, leaves the dielectric layer 204 exposed at the bottom of the trench 212.

In the present invention, following the etch process, a second barrier layer [0019] 220, such as Ta, TaN, TiSiNx, TaSiNx, W, or WNx is sputter deposited using PVD onto the first barrier layer 208 and the exposed dielectric layer at the bottom of the trench 212, as shown in Figure 5. The PVD barrier layer 220 covers the bottom of the trench 212 and the field surface 214. The PVD barrier layer 220 on the bottom of the trench 212 covers the dielectric layer at the bottom of the trench which was previously exposed during the etching process to remove the barrier layer 208 from the bottom of the via 210. The PVD barrier layer 220 may also partially or completely cover the vertical surfaces of the patterned feature, such as the sidewalls 216, 218 of the trench 202 and the via 200, respectively. However, the deposition of the PVD barrier layer 220 is minimized at the bottom of the via 210. At this point in the process, the aspect ratio of the via will typically be in the range of about 4 to 1, and the aspect ratio of the trench will typically be in the range of about 1 to 1. Because of the high aspect ratio/narrow opening of the via 200, few of the atoms or molecules sputtered by PVD will be sputtered at the appropriate angle to reach the bottom of the via 210. High density plasma PVD (HDP-PVD) or other directional PVD techniques may be used to further minimize deposition on the bottom of the via.

[0020] In another embodiment, the second barrier layer is deposited, at least partially, at the bottom of the via (not shown). For example, the barrier layer may have a thickness of from about 20 Å to about 50 Å at the bottom of the via. Preferably, the PVD barrier layer covering the bottom of the via has a low

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[0021] PVD, CVD, or electroless deposition, as shown in Figure 6. A seed layer is a layer on which a subsequent metal layer can be deposited by a process such as PVD, CVD, or electroplating. Copper is deposited on the seed layer by PVD, CVD, or electroplating to fill the trench and via features on the patterned substrate (not shown).

A similar process sequence may be performed on a patterned substrate [0022] with an etch stop, such as a nitride etch stop, at the via level. Figure 7 shows the starting material patterned substrate with an etch stop 224 disposed at the bottom of the feature. The steps of a preferred embodiment of this method are illustrated by Figures 2, 3, 8, and 5. Figure 8 shows that the etch stop 224 is removed from the bottom of the via 210 during the etching step which removes the barrier layer 208 from the bottom of the via 210.

A schematic of a multichamber processing apparatus 35 suitable for [0023] performing the processes of the present invention is illustrated in Figure 9. The apparatus is an "ENDURA" system commercially available from Applied Materials, Santa Clara, California. The particular embodiment of the apparatus 35 shown herein is suitable for processing planar substrates, such as semiconductor substrates, and is provided to illustrate the invention, and should not be used to limit the scope of the invention. The apparatus 35 typically comprises a cluster of interconnected process chambers 36, for example, CVD and PVD deposition and rapid thermal annealing chambers.

The apparatus comprises a CVD deposition chamber 41 (shown in Figure [0024] 10) which is used to deposit the conformal barrier layer 208 in one embodiment. The CVD deposition chamber 41 has surrounding sidewalls 45 and a ceiling 50.

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The chamber 41 comprises a process gas distributor 55 for delivering process gases into the chamber. Mass flow controllers and air operated valves are used to control the flow of process gases into the deposition chamber 41. The gas distributor 55 is typically mounted above the substrate (as shown), or peripherally about the substrate (not shown). A support 65 is provided for supporting the substrate in the deposition chamber 41. The substrate is introduced into the chamber 41 through a substrate loading inlet in the sidewall 45 of the chamber 41 and placed on the support 65. The support 65 can be lifted or lowered by support lift bellows 70 so that the gap between the substrate and gas distributor 55 can be adjusted. A lift finger assembly 75 comprising lift fingers that are inserted through holes in the support 65 can be used to lift and lower the substrate onto the support to facilitate transport of the substrate into and out of the chamber 41. A thermal heater 80 is then provided in the chamber to rapidly heat the substrate. Rapid heating and cooling of the substrate is preferred to increase processing throughput, and to allow rapid cycling between successive processes operated at different temperatures. The temperature of the substrate is generally estimated from the temperature of the support 65.

[0025] The substrate is processed in a process zone 95 above a horizontal perforated barrier plate 105. The barrier plate 105 has exhaust holes 110 which are in fluid communication with an exhaust system 115 for exhausting spent process gases from the chamber 41. A typical exhaust system 115 comprises a rotary vane vacuum pump (not shown) capable of achieving a minimum vacuum of about 10 mTorr, and optionally a scrubber system for scrubbing byproduct gases. The pressure in the chamber 41 is sensed at the side of the substrate and is controlled by adjusting a throttle valve in the exhaust system 115.

[0026] A plasma generator 116 is provided for generating a plasma in the process zone 95 of the chamber 40 for plasma enhanced chemical vapor deposition processes. The plasma generator 116 can generate a plasma (i) inductively by applying an RF current to an inductor coil encircling the deposition chamber (not shown), (ii) capacitively by applying an RF current to process electrodes in the chamber, or (iii) both inductively and capacitively while the chamber wall or other electrode is grounded. A DC or RF current at a power level of from about 750 Watts

to about 2000 Watts can be applied to an inductor coil (not shown) to inductively couple energy into the deposition chamber to generate a plasma in the process zone 95. When an RF current is used, the frequency of the RF current is typically from about 400 KHz to about 16 MHZ, and more typically about 13.56 MHZ Optionally, a gas containment or plasma focus ring (not shown), typically made of aluminum oxide or quartz, can be used to contain the flow of process gas or plasma around the substrate.

[0027] In another embodiment, a conformal barrier layer 208 is formed over the patterned surface by atomic layer deposition (ALD). The ALD barrier layer may be formed from materials such as Ta, TaN, W, or WN. Examples of ALD processes are described in commonly assigned U.S. patent application serial no. 09/754,230, entitled "Method of Forming Refractory Metal Nitride Layers Using Chemisorption Techniques," filed on January 3, 2001, U.S. patent application serial no. 09/960,469, entitled "Formation of Refractory Metal Nitrides Using Chemisorption Techniques," filed on 9/19/01, and U.S. patent application serial no. 09/965,370, entitled "Integration of Barrier Layer and Seed Layer," filed on 9/26/01, which are hereby incorporated by reference.

[0028] Generally, ALD can be used to deposit monolayers of materials, such as monolayers of a nitrogen-based compound and a metal containing compound, which are alternately chemisorbed on a substrate. For example, a monolayer of a nitrogen-based compound is chemisorbed on a substrate by introducing a pulse of a nitrogen-based gas into a processing chamber. After the monolayer is chemisorbed onto the substrate, excess nitrogen-based compound is removed from the processing chamber by introducing a pulse of purge gas thereto. Purge gases, such as, for example, helium (He), argon (Ar), nitrogen (N_2), and hydrogen (N_2), and other gases, may be used. After the pulse of purge gas, a pulse of a metal containing compound is introduced into the processing chamber to chemisorb a monolayer of metal containing compound on the substrate. The metal containing compound may be provided as a gas or may be provided with the aid of a carrier gas. Examples of carrier gases which may be used include, but are not limited to, helium (He), argon (Ar), nitrogen (N_2), and hydrogen (N_2).

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In another embodiment of ALD, instead of using pulses of a purge gas [0029] between the pulses of a nitrogen-based compound and a metal containing compound, the purge gas is continuously flowed, i.e., both during the pulses of a nitrogen-based compound and the pulses of a metal containing compound, and in between these pulses.

One exemplary process of depositing a tantalum nitride barrier layer by atomic layer deposition in a processing chamber comprises sequentially providing pentadimethylamino-tantalum (PDMAT) at a flow rate between about 100 sccm and about 1000 sccm, and preferably between about 200 sccm (standard cubic centimeters per minute) and 500 sccm, for a time period of about 1.0 second or less, providing ammonia at a flow rate between about 100 sccm and about 1000 sccm, preferably between about 200 sccm and 500 sccm, for a time period of about 1.0 second or less, and a purge gas at a flow rate between about 100 sccm and about 1000 sccm, preferably between about 200 sccm and 500 sccm for a time period of about 1.0 second or less. The heater temperature preferably is maintained between about 100°C and about 300°C at a chamber pressure between about 1.0 and about 5.0 torr. This process provides a tantalum nitride layer in a thickness between about 0.5 Å and about 1.0 Å per cycle. The alternating sequence may be repeated until a desired thickness is achieved.

A pre-clean chamber which can be used to remove the barrier layer 208 [0031] from the bottom of the via 210 is the Pre-Clean II chamber available from Applied Materials, Inc. of Santa Clara, California. Additionally, other etch chambers known in the field could be used to remove the barrier layer as described. In a preferred embodiment, the CVD chamber 41 of Figure 16 can be used to etch the CVD barrier layer deposited on the substrate. The support pedestal 82 may be used to bias the substrate. A plasma generator 116, as described above, is attached to the support pedestal 82. Argon is the principal etching gas. It ionizes in the chamber, and its positively charged ions are attracted to the negatively biased substrate with enough energy that the barrier layer 208 is removed from the horizontal surfaces of the patterned feature.

[0032] In another embodiment, the barrier layer 208 may be deposited and then

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removed from the bottom of the via 210 in an ALD chamber with plasma capability.

[0033] A conventional PVD deposition chamber commercially available from Applied Materials, Santa Clara, California can be used to deposit a second barrier layer 220 on a substrate. Figure 11 shows a simplified example of a PVD chamber 300. The PVD chamber 300 generally includes a chamber section 306. The chamber section 306 generally includes a substrate support member 302 for supporting a substrate (not shown) to be processed, a target 304 for providing a material to be deposited on the substrate and a process environment 303 wherein a plasma is created for ions to sputter the target 304.

The PVD chamber 300 generally includes the substrate support member 302, also known as a susceptor or heater, disposed within the chamber section 306. The substrate support member 302 may heat the substrate if required by the process being performed. A target 304 is disposed in the top of the chamber section 306 to provide material, such as aluminum, titanium or tungsten, to be sputtered onto the substrate during processing by the PVD chamber 300. A lift mechanism, including a guide rod 326, a bellows 328 and a lift actuator 330 mounted to the bottom of the chamber section 306, raises the substrate support member 302 to the target 304 for the PVD chamber 300 to perform the process and lowers the substrate support member 302 to exchange substrates. A set of shields 332, 334, 336, disposed within the chamber section 306, surround the substrate support member 302 and the substrate during processing in order to prevent the target material from depositing on the edge of the substrate and on other surfaces inside the chamber section 306.

[0035] Situated above the chamber section 306 and sealed from the processing region of the chamber is a cooling chamber 316. The cooling chamber 316 is generally defined by the target 304, a top 317 and sides 319. A cooling fluid, such as water or antifreeze, flows into the cooling chamber 316 through inlet 318 and out of the cooling chamber 316 through outlet 320.

[0036] A rotating magnetron 308 is disposed in the cooling chamber 316 on the non-process environment side of the target 304 and surrounded by the cooling fluid. The magnetron 308 is isolated from the vacuum in the chamber section 306 by seals

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(not shown) between the magnetron chamber and target and between the target and processing region. The magnetron 308 has a set of magnets 310 arranged within the magnetron 308 so that they create magnetic field lines spinning across the sputtering surface of the target. Electrons are captured along these lines, where they collide with gas atoms, creating ions. To create this effect about the circumference of the target, the target is rotated during processing. The magnetron 308 is situated above the top side of the target 304 with about a one millimeter gap therebetween, so the magnetic fields from the magnets 310 may penetrate through the target 304. A motor assembly 312 for rotating the magnetron 308 is mounted to the top 317 of the cooling chamber 316. A shaft 314, which mechanically couples the motor assembly 312 to the rotational center of the magnetron 308, extends through the top 317. The motor assembly 312 imparts a rotational motion to the magnetron 308 to cause it to spin during performance of the substrate process.

[0037] A negative DC bias voltage of about 200 V or more is typically applied to the target 304, and a ground is applied to an anode, the substrate support member 302, and the chamber surfaces. The combined action of the dc bias and the rotating magnetron 308 generate an ionized plasma discharge in a process gas, such as argon, between the target 304 and the substrate. The positively charged ions are attracted to the target 304 and strike the target 304 with sufficient energy to dislodge atoms of the target material, which sputters onto the substrate.

[0038] The process can be implemented using a computer program product that runs on a conventional computer system comprising a central processor unit (CPU) interconnected to a memory system with peripheral control components, such as for example a 68400 microprocessor, commercially available from Synenergy Microsystems, California.

Example 1

In one example, a process according to the present invention was [0039] performed on a substrate having a 0.25 µm via with about a 4:1 aspect ratio and a trench. The patterned substrate was first introduced into a CVD chamber, such as a Express Mail No. EV041916406US

TxZ® chamber, commercially available from Applied Materials, Inc., Santa Clara, California, where about 50 Å to about 100 Å of SixNy was deposited on the substrate using CVD techniques. The substrate was then moved into a Pre-clean II chamber (available from Applied Materials, Inc., located in Santa Clara, California), where the substrate was subjected to an argon/hydrogen etching environment for about 20 seconds. RF/DC powers of about 300/300W were used. Next, the substrate was moved into a PVD chamber where about 400 Å of TaN was deposited on the substrate in the field. Next, the substrate was introduced into a CVD chamber where about 400 Å of CVD Cu was deposited on the substrate as a wetting layer. Then, Cu was sputtered onto the substrate to complete the fill the via and the trench.

Example 2

[0040] In another example, a patterned substrate with a dual damascene trench structure and a via opened to an underlying Cu wiring was first introduced into a multichamber processing apparatus having a sputter clean chamber, a CVD barrier chamber, a PVD barrier chamber, and a PVD Cu chamber. 50 Å of TiSixN was deposited on the substrate in a CVD barrier chamber at a pressure of less than 10 Torr and at a temperature of about 300°C to about 380°C by reacting TDMAT in a N₂/H₂ environment to form a plasma. The substrate was then treated with a SiH₄ soak. The deposited TiSi_xN conformally covered both the via and trench structure. In the next step, the substrate was moved to the sputter clean chamber, and subjected to argon/hydrogen etch to etch off the TiSixN film deposited at the bottom of the via. The etching was continued past the bottom of the via into the underlying Cu wiring to remove about 5 to 10 Å of the underlying Cu wiring. The etch process also removed the TiSixN film at the bottom of the trench structure. Next, the substrate was moved into a PVD Ta/TaN chamber to receive a Ta/TaN film having a thickness at the bottom of the trench structure of about 30 Å. Then, the substrate was transferred into a PVD Cu chamber where about 1500 Å of Cu was deposited on the substrate with minimal deposition at the bottom of the via.

While the foregoing is directed to the preferred embodiment of the present [0041] invention, other and further embodiments of the invention may be devised without

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departing from the basic scope thereof, and the scope thereof is determined by the claims which follow.

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What is claimed is:

1. A method of filling one or more of a via and a trench in a patterned substrate, comprising:

- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition;
- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
- c) depositing a second barrier layer by physical vapor deposition; and then
 - d) depositing one or more conductive materials.
- 2. The method of claim 1 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.
- 3. The method of claim 2 wherein the first barrier layer is selected from the group consisting of Si_xN_y, TiSi_xN, TiN(C), TiNSi(C), Ta, TaC, TaN(C), TaNSi(C), W, WN_x, SiO_xN_y, SiC, AlN, and Al₂O₃.
- 4. The method of claim 3 wherein the second barrier layer is selected from the group consisting of Ta, TaN, TiSiN_x, TaSiN_x, W, and WN_x.
- 5. The method of claim 4 wherein the seed layer is copper.
- 6. The method of claim 5 wherein the metal layer is copper.
- 7. The method of claim 1 wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.
- 8. The method of claim 7 wherein the chamber is a chemical vapor deposition

The method of claim 2 wherein the seed layer is deposited by physical vapor 9. deposition.

The method of claim 2 wherein the seed layer is deposited by chemical vapor 10.

deposition.

The method of claim 2 wherein the seed layer is deposited by electroless 11.

deposition.

The method of claim 2 wherein the metal layer is deposited by physical vapor 12.

deposition.

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The method of claim 2 wherein the metal layer is deposited by chemical 13.

vapor deposition.

The method of claim 2 wherein the metal layer is deposited by electroplating. 14.

The method of claim 1 wherein the via has an aspect ratio of about 4 to 1 and 15.

the trench has an aspect ratio of about 1 to 1.

The method of claim 1 wherein the second barrier layer has a thickness of 16.

from about 20 Å to about 50 Å at the bottom of the via.

17. The method of claim 1 wherein the second barrier layer is selected from the

group consisting of Ta, TaN, W, WNx, Ti, and TiN, and the second barrier layer has

a thickness of from about 20 Å to about 50 Å at the bottom of the via.

A method of filling one or more of a via and a trench in a patterned substrate,

comprising:

depositing a generally conformal first barrier layer on the patterned a)

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substrate by atomic layer deposition;

b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;

depositing a second barrier layer by physical vapor deposition; and C) then

d) depositing one or more conductive materials.

19. The method of claim 18 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.

The method of claim 19 wherein the first barrier layer is selected from the 20. group consisting of Ta, TaN, W, and WN.

The method of claim 20 wherein the second barrier layer is selected from the 21. group consisting of Ta, TaN, TiSiNx, TaSiNx, W, and WNx.

22. The method of claim 21 wherein the seed layer is copper.

The method of claim 22 wherein the metal layer is copper. 23.

24. The method of claim 18 wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool.

The method of claim 24 wherein the chamber is an atomic layer deposition 25. chamber and the first barrier layer is deposited and etched in the chamber.

The method of claim 19 wherein the seed layer is deposited by physical vapor 26. deposition.

27. The method of claim 19 wherein the seed layer is deposited by chemical A CONTROL OF THE PARTY OF THE P

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vapor deposition.

28. The method of claim 19 wherein the seed layer is deposited by electroless deposition.

29. The method of claim 19 wherein the metal layer is deposited by physical vapor deposition.

- 30. The method of claim 19 wherein the metal layer is deposited by chemical vapor deposition.
- 31. The method of claim 19 wherein the metal layer is deposited by electroplating.
- 32. The method of claim 18 wherein the via has an aspect ratio of about 4 to 1 and the trench has an aspect ratio of from about 1 to about 1.
- 33. The method of claim 18 wherein the second barrier layer has a thickness of from about 20 Å to about 50 Å at the bottom of the via.
- 34. The method of claim 18 wherein the second barrier layer is selected from the group consisting of Ta, TaN, W, WN_x, Ti, and TiN, and the second barrier layer has a thickness of from about 20 $\rm \mathring{A}$ to about 50 $\rm \mathring{A}$ at the bottom of the via.
- 35. A method of filling one or more of a via and a trench in a patterned substrate having an etch stop at the via level, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition;
 - b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) removing the etch stop from the bottom of the via;
 - d) depositing a second barrier layer by physical vapor deposition; and

Attorney Docket No.: AMAT/1931.P1/CPI/ALUMINUM/PJS

Express Mail No. EV041916406US

then

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e) depositing one or more conductive materials.

36. The method of claim 35 wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.

- 37. A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition;
- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer; and then
 - d) depositing one or more conductive materials.
- 38. A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition;
- b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer; and then
 - d) depositing one or more conductive materials.
- 39. An integrated processing tool, comprising:

Attorney Docket No.: AMAT/1931.P1/CPI/ALUMINUM/PJS

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a central transfer chamber having a robot assembly disposed at least partially therein for moving substrates;

an chemical vapor deposition chamber for depositing and etching a first barrier layer; and

a physical vapor deposition chamber for depositing a second barrier layer.

40. An integrated processing tool, comprising:

a central transfer chamber having a robot assembly disposed at least partially therein for moving substrates;

an atomic layer deposition chamber for depositing and etching a first barrier layer; and

a physical vapor deposition chamber for depositing a second barrier layer.

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ABSTRACT OF THE DISCLOSURE

Embodiments of the present invention provide a process sequence and related hardware for filling a patterned feature on a substrate with a metal, such as copper. The sequence comprises first forming a reliable barrier layer in the patterned feature to prevent diffusion of the metal into the dielectric layer through which the patterned feature is formed. One sequence comprises forming a generally conformal barrier layer over a patterned dielectric, etching the barrier layer at the bottom of the patterned feature, depositing a second barrier layer, and then filling the patterned feature with a metal, such as copper.

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AMAT/1931 P1/CPI/ALUMINUM/PJS

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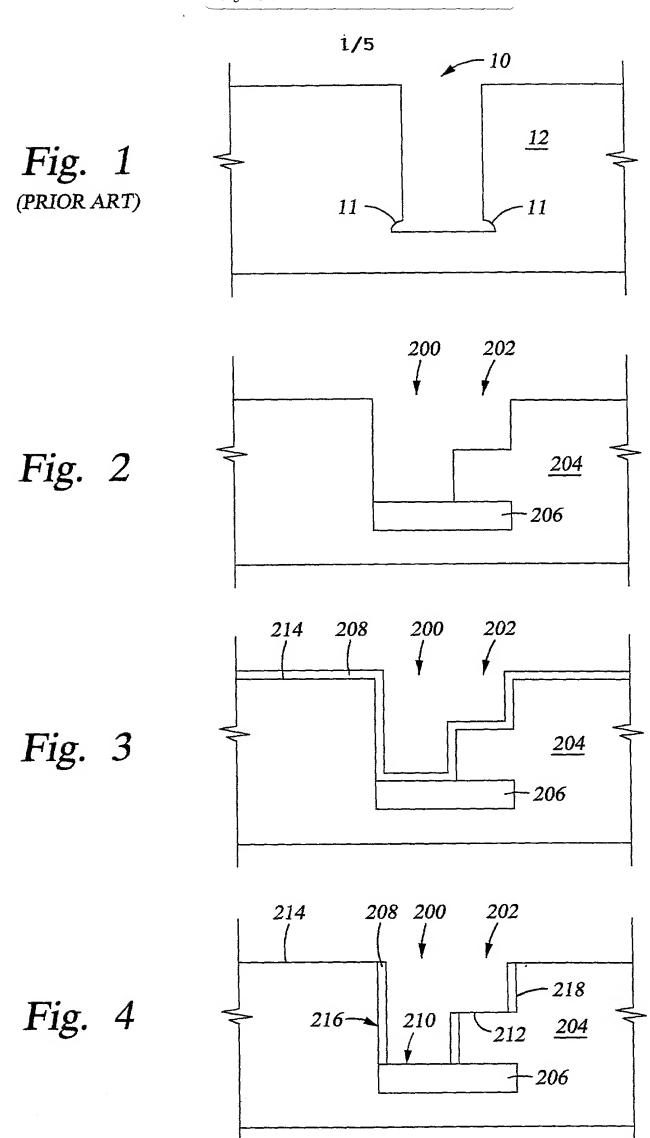
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Applicant:

HEREWITH APPLIED MATIERALS, INC.

Inventor: XI, ET AL. Express Mail No.: EV041916406US

Page 1 of 5



AMAT/1931.P1/CPI/ALUMINUM/PJS Atty Dkt. No. UNKNOWN HEREWITH U.S. Serial No. Filed: APPLIED MATIERALS, INC. XI, ET AL. Applicant: Inventor: Express Mail No.: EV041916406US Page 2 of 5 2/5 220 202 208 200 214 218 Fig. 5 216-210 204 212 206 202 208 200 222 220 214 Fig. 6 204 -206 200 202 <u>204</u> 224 Fig. 7 206 200 202 214 208 218 212 216-204 210 224 Fig. 8 206

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Atty Dkt. No.

AMAT/1931.PI/CPI/ALUMINUM/PJS UNKNOWN HEREWITH APPLIED MATIERALS, INC.

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U.S. Serial No. Filed:

Applicant:

Inventor:

XI, ET AL.

Express Mail No.: EV041916406US Page 3 of 5

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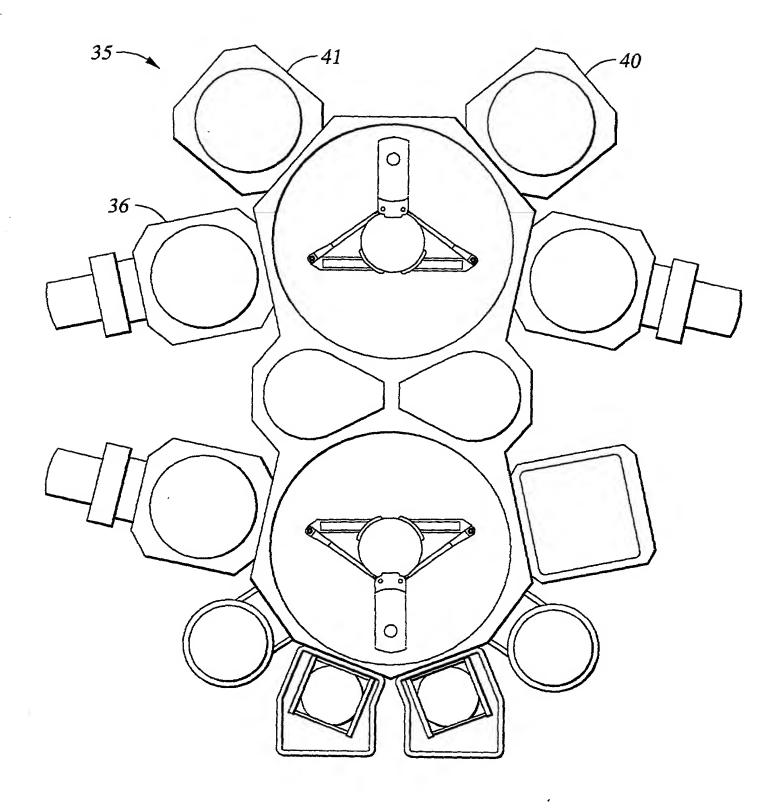
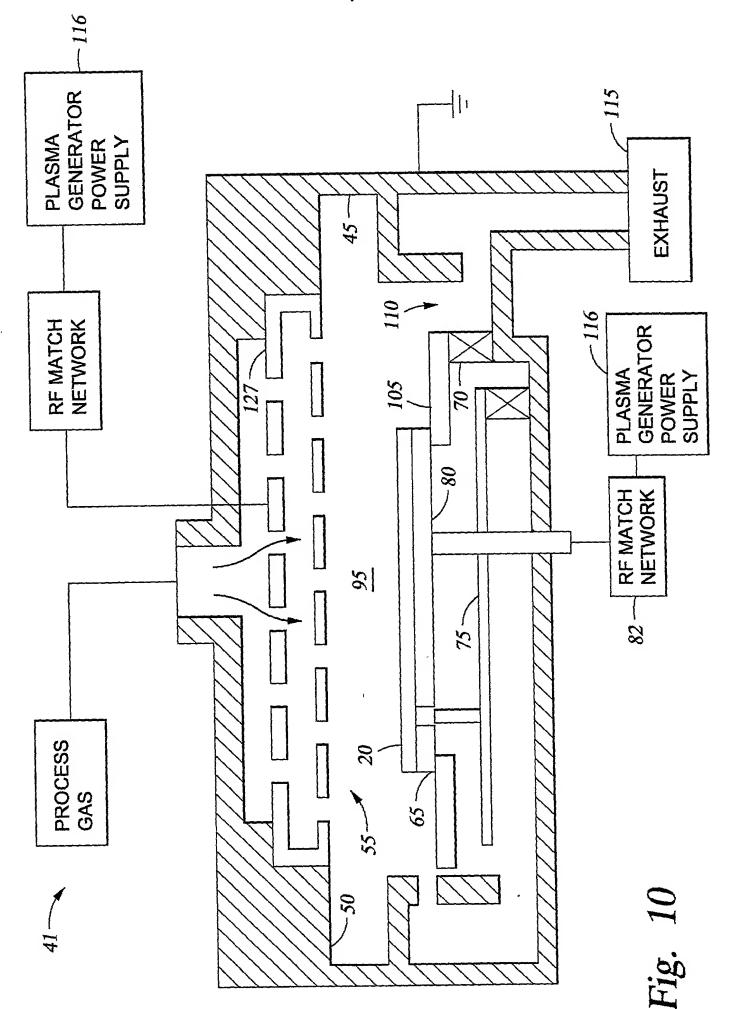


Fig. 9

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Filed: HEREWITH
Applicant: APPLIED MATIERALS, INC.
Inventor: XI, ET AL.
Express Mail No.: EV041916406US
Page 4 of 5

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Atty Dkt. No.

AMAT/1931.P1/CPI/ALUMINUM/PJS

UNKNOWN HEREWITH U.S. Serial No. Filed:

Applicant:

APPLIED MATIERALS, INC. XI, ET AL.

Inventor: Express Mail No.: EV041916406US Page 5 of 5

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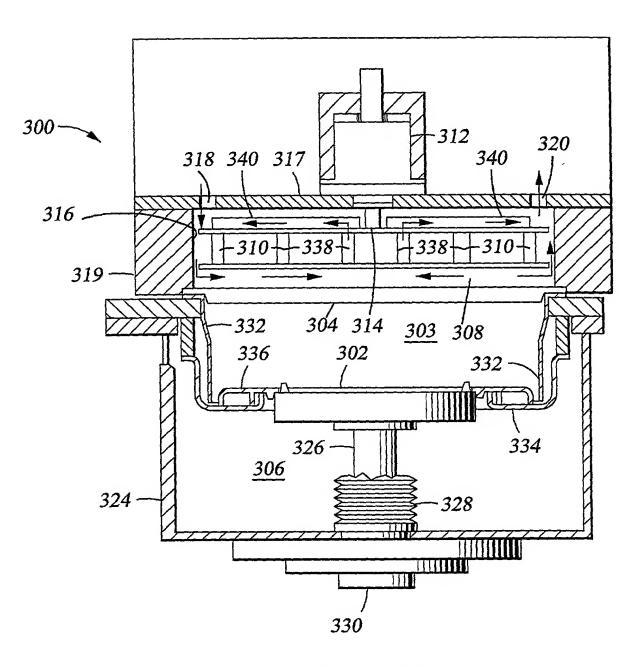


Fig. 11

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

This declaration	is of the following type:
[] [] [X]	original divisional continuation continuation-in-part

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

SPECIFICATION IDENTIFICATION

The specification of which:

[^]	is attached hereto
[]	was filed on , under Serial No. , executed on even date herewith; or
[]	Express Mail No.(as Serial No. not yet known)
	and was amended on (if applicable)
[]	was described and claimed in PCT International Application No
	filed on and as amended under PCT Article 19 on

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with

Title 37, Code of Federal Regulations, 1.56, and which is material to the examination of this application; namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

[] In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. 119)

I hereby claim foreign priority benefits under Title 35, United States Code, 119, of any provisional or foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any provisional or foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

filed by		the sar	n(s) designating ne subject matte					
	[X]	No su	ch applications h	ave been filed.				
	[]	Such a	applications have	been filed as t	follows:			
A.	Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to the application, and any priority claims under 35 U.S.C. 119							to this
	Coun	try/PCT	Application	n No	Date Filed		Priority Clair	med
							[] Yes [] [] Yes [] [] Yes []	No
В.	All fore U.S. ap		olication(s), if an	ny, filed more	than 12 mos. (6 mos for	design) prior	to this
	Country Applications Filing date	tion No:						
C.	U.S. Pr	ovision	al Application f	iled within 12	months prior t	o this app	lication	
	Serial N	<u>ło.</u>		<u>Filing</u>	Date			
			PRI	ORITY CLAIM	(35 U.S.C. 120))		
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	[] [X]		h applications ha pplications have		follows:			
	Serial N	<u>o</u> .	Filing Date	Patented	Pending	Status _ Aband		
	08/856,	116	May 14, 1997		Pending			

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Send correspondence to:

Direct telephone calls to:

Patent Counsel Applied Materials, Inc. P.O. Box 450-A Santa Clara, CA 95052

B. Todd Patterson
MOSER, PATTERSON & SHERIDAN, L.L.P.

713-623-4844

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

ruii name of first inven	tor: MING XI					
Inventor's signature: Residence:	138 Beaumere Way Milpitas, CA 95035	Date: <i> </i>	102			
Post Office Address:	SAME AS ABOVE U.S.A.	Country of Citizenship:	P.R. CHINA			
Full name of second inventor: PAUL FREDERICK SMITH						
Inventor's signature:		Date:				
Residence:	225 E. Taylor Street #4 San Jose, CA 95112					
Post Office Address:	SAME AS ABOVE U.S.A.	Country of Citizenship:	IISA			

Full name of third inventor:	LING CHEN		
Inventor's signature:		Date:	
Residence:	784 Dartshire Way	Dato	
	Sunnyvale, CA 94087		
Post Office Address:	SAMÉ AS ABOVE		
	U.S.A.	Country of Citizenship:	P.R. CHINA
Cull name of facults in contact	MOUATLY VANO		
Full name of fourth inventor:	MICHAEL X. YANG		F
Inventor's signature:	<u>`</u>	Date: 1/K	0/2002
Residence:	793 Cereza Drive	Date (/ ·	
	Paio Alto, CA 94306		
Post Office Address:	SAME AS ABOVE		
	U.S.A.	Country of Citizenship:	P.R. CHINA
	•		
Full name of fifth inventor:	MELOUANIO		
rui name of min inventor:	MEI CHANG		
Inventor's signature:		Date:	
Residence:	12881 Corte de Arguell		
	Saratoga, CA 95070		
Post Office Address:	SAME AS ABOVE		
	U.S.A.	Country of Citizenship:	USA
Full name of sixth inventor:	FUSEN CHEN		
i di name di sixti mventor.	I OGEN OFFER		
Inventor's signature:		Date:	
Residence:	10390 Stern Avenue		
	Cupertino, CA 95014		
Post Office Address:	SAME AS ABOVE		
	U.S.A.	Country of Citizenship:	TAIWAN
Full name of seventh inventor:	CHRISTOPHE MARCA	DAI	
Inventor's signature:	· · · · · · · · · · · · · · · · · · ·	Date:	
Residence:	3655 Proneridge Avenu	ıe #124	
David Office Addition	Santa Clara, CA 95051		
Post Office Address:	SAME AS ABOVE		
	U.S.A.	Country of Citizenship:	FRANCE
Full name of eighth inventor:	JENNY C. LIN		
Inventor's signature:		Date:	
Residence:	12725 Miller Avenue		
Doot Office Address	Saratoga, CA 95070		
Post Office Address:	SAME AS ABOVE	Carmin, of Ottle	LICA
	U.S.A.	Country of Citizenship:	NOA

(Declaration ends with this page)

COMBINED DECLARATION AND POWER OF ATTORNEY

As	а	below	named	invent	or, i	here	ру с	lec	lare	tha	at
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I his declaratio	I his declaration is of the following type:					
[] [] [X]	original divisional continuation continuation-in-part					
	INVENTORSHIP IDENTIFICATION					
My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:						
	RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION					
	SPECIFICATION IDENTIFICATION					
The specification	on of which:					
[] [] [x]	is attached hereto was filed on , under Serial No. , executed on even date herewith; or Express Mail No.(as Serial No. not yet known) and was amended on (if applicable) was described and claimed in PCT International Application No filed on and as amended under PCT Article 19 on					
	ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR					
I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.						
I acknowledge with	the duty to disclose all information I know to be material to patentability in accordance					
Title 37, Code application; nat	of Federal Regulations, 1.56, and which is material to the examination of this mely, information where there is a substantial likelihood that a reasonable Examiner it important in deciding whether to allow the application to issue as a patent, and					
[]	In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR 1.98.					

PRIORITY CLAIM (35 U.S.C. 119)

I hereby claim foreign priority benefits under Title 35, United States Code, 119, of any provisional or foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any provisional or foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

	[X]	No such applications have been filed.					
	[]	Such app	lications have	e been filed a	as follows:		
A.					ithin 12 mos. (6 er 35 U.S.C. 119	mos. for design) prior to this	
	Coun	try/PCT	Application	n No	Date Filed	Priority Claimed	
						[] Yes [] No [] Yes [] No [] Yes [] No	
B.		ign applic	ation(s), if a	ny, filed mo	re than 12 mos. (6	6 mos for design) prior to this	
	Country Applica Filing da	tion No:					
C.	U.S. Pr	ovisional A	Application f	iled within	12 months prior to	this application	
	Serial N	<u>10.</u>		<u>Fil</u>	ing Date		
			PRI	ORITY CLA	IM (35 U.S.C. 120)		
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	[] [X]	No such applications have been filed Such applications have been filed, as follows:					
	<u>Serial N</u>	<u>o</u> . <u>Fi</u>	ling Date	Patented	Pending	Status Abandoned	
		116 Ma	ay 14, 1997		Pending		

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Michael L. Sherrard Raymond Kam-On Kwong James C. Wilson Robert W. Mulcahy Walter Benjamin Glenn B. Todd Patterson Raymond R. Moser, Jr. Keith M. Tackett	Registration No. 28,041 Registration No. 37,165 Registration No. 35,412 Registration No. 25,436 Registration No. 44,713 Registration No. 37,906 Registration No. 34,682 Registration No. 32,008
	Registration No. 32,008 Registration No. 32,982
Transcrib. Latte15011	Registration No. 34,102

Send correspondence to:

Direct telephone calls to:

Patent Counsel Applied Materials, Inc.

P.O. Box 450-A
Santa Clara, CA 95052

B. Todd Patterson

MOSER, PATTERSON & SHERIDAN, L.L.P.

713-623-4844

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Full name of first inver	ntor: MING XI	
Inventor's signature:		Date:
Residence:	138 Beaumere Way	
Post Office Address:	Milpitas, CA 95035 SAME AS ABOVE	
	U.S.A.	Country of Citizenship: P.R. CHINA
Inventor's signature:	ran Rederick Su	MITH Date: 01/10/02
Residence:	225 E. Taylor Street #4 San Jose, CA 95112	
Post Office Address:	SAME AS ABOVE	Country of Citizenship: USA
	955 Stonehust Way Campbell, CA, 9500	oralization p. Ody
	Campbell, CA, 9500	8

Full name of third inventor:	LING CHEN			
Inventor's signature:		Data:		
Residence:	784 Dartshire Way	Date:		
	Sunnyvale, CA 94087			
Post Office Address:	SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	P.H. CHINA	
Full name of fourth inventor:	MICHAEL X. YANG			
Inventoria signatura.	Date:			
Inventor's signature: Residence:	793 Cereza Drive	Date:		
1.55.45/1001	Palo Alto, CA 94306			
Post Office Address:	SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	P.R. CHINA	
Full name of fifth inventor:	MEI CHANG			
	_			
Inventor's signature: Residence:				
riesiderice.	12881 Corte de Arguelle Saratoga, CA 95070	U		
Post Office Address:	SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	USA	
Full name of sixth inventor:	FUSEN CHEN			
Inventor's signature:Residence:	10200 Storn Avenue	Date:		
residence.	10390 Stern Avenue Cupertino, CA 95014			
Post Office Address:	SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	TAIWAN	
Full name of seventh inventor:	CHRISTOPHE MARCADAL			
Inventor's signature:	0055 D	Date:		
Residence:	3655 Proneridge Avenu Santa Clara, CA 95051	e #124		
Post Office Address:	SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	FRANCE	
Full name of eighth inventor:	JENNY C. LIN			
t di namo di digital involtor.	OLIMIT O. LIM			
Inventor's signature:		Date:		
Residence:	12725 Miller Avenue			
Post Office Address:	Saratoga, CA 95070 SAME AS ABOVE			
	U.S.A.	Country of Citizenship:	USA	

(Declaration ends with this page)

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inve	ntor, I here	by dec	lare that:
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This declaration is of the following type:

[] di [] co	riginal ivisional ontinuation ontinuation-in-part			
INVENTORSHIP IDENTIFICATION				
the original, first a	st office address and citizenship are as stated below next to my name. I believe I am and sole inventor (if only one name is listed below) or an original, first and joint names are listed below) of the subject matter which is claimed and for which a patent evention entitled:			
l	RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION			
	SPECIFICATION IDENTIFICATION			
The specification of	of which:			
[] wa [] Ex an [] wa	attached hereto as filed on , under Serial No. , executed on even date herewith; or xpress Mail No.(as Serial No. not yet known) nd was amended on (if applicable) as described and claimed in PCT International Application No ed on and as amended under PCT Article 19 on			
ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR				
	I have reviewed and understand the contents of the above-identified specification, s, as amended by any amendment referred to above.			
I acknowledge the with	duty to disclose all information I know to be material to patentability in accordance			
Title 37, Code of application; namely	f Federal Regulations, 1.56, and which is material to the examination of this ly, information where there is a substantial likelihood that a reasonable Examiner apportant in deciding whether to allow the application to issue as a patent, and			
	compliance with this duty there is attached an Information Disclosure Statement in cordance with 37 CFR 1.98.			

	[X]	No sucl	No such applications have been filed.						
	[]	Such a	oplications ha	ve been file	ed as fo	llows:			
A.			CT applicat d any priorit				6 mos. for	design) prid	or to this
	Coun	try/PCT	<u>Applicat</u>	ion No		Date Filed		Priority Cla	aimed
								[] Yes [[] Yes [[] Yes [No
В.		ign appl plication		any, filed	more th	an 12 mos.	(6 mos for	design) pric	or to this
	Country Applica Filing d	tion No:							
C.	U.S. Pr	ovisiona	ıl Applicatio	n filed with	in 12 m	onths prior	to this app	olication	
	Serial I	<u> 10.</u>			Filing Date				
			P	RIORITY	CLAIM (35 U.S.C. 12	0)		
or PCT and, ins prior ap I ackno (namely importa	internates of ar as explication owledge by, informatin decay ag date	tional appoint appoint and the subject of the subje	clication(s) det matter of emanner proto to disclose in the term is settler to allo	esignating each of the vided by the nformation ubstantial liw the appli	the Unit claims e first path that is kelihoodication to	ted States or of this applications of a material to the distinction that a reason o issue as a	f America tation is not Fitle 35, Under the examinationable Ex	ed States app that is/are list disclosed in the lited States Control ation of this a miner would control onal filing da	ted below that/those code, 112, application consider it between
	[] [X]		applications plications ha			llows:			
	Serial N	lo.	Filing Date	Patente		Pending	Status	doned	
	08/856,		May 14, 199		<u>~~</u>	Pending	ADUIT	<u>aorioa</u>	

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Donald Verplancken Michael B. Einschlag Peter J. Sgarbossa Lawrence Edelman Michael L. Sherrard Raymond Kam-On Kwong James C. Wilson Robert W. Mulcahy Walter Benjamin Glenn B. Todd Patterson Raymond R. Moser, Jr. Keith M. Tackett Douglas H. Elliott	Registration No. 33,217 Registration No. 29,301 Registration No. 25,610 Registration No. 25,226 Registration No. 28,041 Registration No. 37,165 Registration No. 35,412 Registration No. 25,436 Registration No. 44,713 Registration No. 37,906 Registration No. 34,682 Registration No. 32,008 Registration No. 32,008
Douglas H. Elliott William B. Patterson	-

Send correspondence to:

Direct telephone calls to:

Patent Counsel Applied Materials, Inc. P.O. Box 450-A Santa Clara, CA 95052

B. Todd Patterson MOSER, PATTERSON & SHERIDAN, L.L.P.

713-623-4844

DECLARATION

Full name of first inventor: MING XI					
Inventor's signature:		Date:			
Residence:	138 Beaumere Way Milpitas, CA 95035				
Post Office Address:	SAME AS ABOVE				
	U.S.A.	Country of Citizenship:	P.R. CHINA		
Full name of second inventor: PAUL FREDERICK SMITH					
Inventor's signature:		Date:			
Residence:	225 E. Taylor Street #4				
Post Office Address:	San Jose, CA 95112 SAME AS ABOVE				
	U.S.A.	Country of Citizenship:	USA		

Full name of third inventor:	LING CHEN		
Inventor's signature:	784 Dartshire Way	Date: 1-10-	01
Post Office Address:	Sunnyvale, CA 94087 SAME AS ABOVE U.S.A.	Country of Citizenship:	P.R. CHINA
Full name of fourth inventor:	MICHAEL X. YANG		
Inventor's signature:Residence:	793 Cereza Drive	Date:	
Post Office Address:	Paio Alto, CA 94306 SAME AS ABOVE U.S.A.	Country of Citizenship:	P.R. CHINA
Full name of fifth inventor:	MEI CHANG		
Inventor's signature:		Date:	
Residence:	12881 Corte de Arguelle	0	
Post Office Address:	Saratoga, CA 95070 SAME AS ABOVE U.S.A.	Country of Citizenship:	USA
Full name of sixth inventor:	FUSEN CHEN		
Inventor's signature:		Date:	
Residence:	10390 Stern Avenue		<u> </u>
Post Office Address:	Cupertino, CA 95014 SAME AS ABOVE U.S.A.	Country of Citizenship:	TAIWAN
Full name of seventh inventor:	CHRISTOPHE MARCAI	DAL	
Inventor's signature:		Date:	
Residence: Post Office Address:	3655 Proneridge Avenue Santa Clara, CA 95051 SAME AS ABOVE U.S.A.	e #124 Country of Citizenship:	
Full name of eighth inventor:	JENNY C. LIN		
Inventor's signature:		_ Date:	
Residence: Post Office Address:	12725 Miller Avenue Saratoga, CA 95070 SAME AS ABOVE U.S.A.		
	J.J.A.	Country of Citizenship:	USA

As a below named inventor, I hereby declare that:

This declaration	is of the following type:
[]	original
[]	divisional
[]	continuation
[X]	continuation-in-part

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My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

SPECIFICATION IDENTIFICATION

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[X]	is attached hereto
[]	was filed on , under Serial No. , executed on even date herewith; or
[]	Express Mail No.(as Serial No. not yet known)
	and was amended on (if applicable)
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priority	is claimed.				
	[X] No	such applications	s have been filed		
	[] Su	ch applications ha	ave been filed as	follows:	
A.	Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to application, and any priority claims under 35 U.S.C. 119				
	Country/F	PCT Applicat	ion No	Date Filed	Priority Claimed
					[] Yes [] No [] Yes [] No [] Yes [] No
В.	All foreign U.S. applic	-	any, filed more	than 12 mos. (6	mos for design) prior to this
	Country: Application Filing date:	No:			
C.	U.S. Provis	ional Applicatio	n filed within 12	months prior to	this application
	Serial No.		<u>Filin</u>	g Date	
		F	PRIORITY CLAIM	l (35 U.S.C. 120)	
or PCT and, ins prior ap I ackno (namely importa	international sofar as the sopplication(s) is whether the sylin in deciding date of the sylin in deciding date of the sylin in the syli	Il application(s) desubject matter of in the manner produty to disclose in where there is so	esignating the Ueach of the claim vided by the first information that is ubstantial likelihow the application	Inited States of a is of this applicate paragraph of Tiles is material to the bod that a reason in to issue as a p	any United States application(s) America that is/are listed below ion is not disclosed in that/those tle 35, United States Code, 112, e examination of this application hable Examiner would consider it batent) which occurred between international filing date of this
		such applications ch applications ha		follows:	
	Serial No.	Filing Date	Patented	Pending	Status Abandoned
	08/856,116	May 14, 199	7	Pending	

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Send correspondence to:

Direct telephone calls to:

Patent Counsel Applied Materials, Inc. P.O. Box 450-A Santa Clara, CA 95052

B. Todd Patterson
MOSER, PATTERSON & SHERIDAN, L.L.P.

713-623-4844

DECLARATION

Truit Haine Of HISLINVE	itor: MING XI					
Inventor's signature: Residence: 138 Beaumere Way Milpitas, CA 95035		Date:				
					Post Office Address:	SAME AS ABOVE
	U.S.A.	Country of Citizenship:	P.R. CHINA			
Full name of second in	Full name of second inventor: PAUL FREDERICK SMITH					
Inventor's signature:		Date:				
Residence:	225 E. Taylor Street #4					
Post Office Address:	San Jose, CA 95112 SAME AS ABOVE U.S.A.	Country of Old				
	U.U.A.	Country of Citizenship	HSA			

Full name of third inventor:	LING CHEN				
Inventor's signature: Residence:	784 Dartshire Way	Date:			
Post Office Address:	Sunnyvale, CA 94087 SAME AS ABOVE U.S.A.	Country of Citizenship: P.R. CHINA			
Full name of fourth inventor:	MICHAEL X. YANG				
Inventor's signature:		Date:			
Residence:	793 Cereza Drive Palo Alto, CA 94306				
Post Office Address:	SAME AS ABOVE U.S.A.	Country of Citizenship: P.R. CHINA			
Full name of fifth inventor:	MEI CHANG				
Inventor's signature:	W Chy	Date: Jan 15 02			
Residence: Post Office Address:	12881 Corte de Argúell Saratoga, CA 95070 SAME AS ABOVE U.S.A.	o Country of Citizenship: USA			
Full name of sixth inventor:	FUSEN CHEN				
Inventor's signature:		Date:			
	10390 Stern Avenue Cupertino, CA 95014 SAME AS ABOVE U.S.A.	Country of Citizenship: TAIWAN			
Full name of seventh inventor:	CHRISTOPHE MARCA	DAL			
Inventor's signature:		Date:			
Residence: Post Office Address:	3655 Proneridge Avenu Santa Clara, CA 95051 SAME AS ABOVE U.S.A.	ie #124			
Full name of eighth inventor:	JENNY C. LIN				
Inventor's signature:	40705 149	Date:			
Residence: Post Office Address:	12725 Miller Avenue Saratoga, CA 95070 SAME AS ABOVE U.S.A.	Country of Citizenship: USA			

As a below named inventor, I hereby declare that:

This declaration is of the following type:				
[] [] [X]	original divisional continuation continuation-in-part			
	INVENTORSHIP IDENTIFICATION			
the original, firs	oost office address and citizenship are as stated below next to my name. I believe I am at and sole inventor (if only one name is listed below) or an original, first and joint all names are listed below) of the subject matter which is claimed and for which a patent invention entitled:			
	RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION			
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A.			CT application				mos. for design) prior to this
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							[] Yes [] No [] Yes [] No [] Yes [] No
В.		ign appli plication		ny, filed r	nore th	an 12 mos. (6 mos for design) prior to this
	Country Applicat Filing da	tion No:					
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	Serial N	<u>lo.</u>			Filing I	<u>Date</u>	
			PRI	ORITY C	LAIM (3	5 U.S.C. 120)
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	[] [X]		applications have			llows:	
	Serial N	·	Filing Date	Patente		Pending	Status
				<u>r-aleme</u>	u		<u>Abandoned</u>
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B. Todd Patterson MOSER, PATTERSON & SHERIDAN, L.L.P.

713-623-4844

Santa Clara, CA 95052

DECLARATION

Full name of first inver	ntor: MING XI		
Inventor's signature:		Date:	
Residence:	138 Beaumere Way Milpitas, CA 95035		
Post Office Address:	SAME AS ABOVE U.S.A.	Country of Citizenship:	P.R. CHINA
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Residence:	12881 Corte de Arguello		
Post Office Address:	Saratoga, CA 95070 SAME AS ABOVE U.S.A.	Country of Citizenship:	USA
Full name of sixth inventor:	FUSEN CHEN	- /	. /
Inventor's signature:	10390 Stern Avenue	Date:	102
Post Office Address:	Cupertino, CA 95014 SAME AS ABOVE U.S.A.	Country of Citizenship:	TAIWAN
Full name of seventh inventor:	CHRISTOPHE MARCAI	DĄL	
Inventor's signature:		Date:	
Residence:	3655 Proneridge Avenue	e #124	
Post Office Address:	Santa Clara, CA 95051 SAME AS ABOVE U.S.A.	Country of Citizenship: 1	FRANCE
Full name of eighth inventor:	JENNY C. LIN		
Inventor's signature:		_ Date:	
Residence:	12725 Miller Avenue		
Post Office Address:	Saratoga, CA 95070 SAME AS ABOVE U.S.A.	Country of Citizenship: \text{\chi}	JSA

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	Serial N	<u>lo.</u>		Fili	ng Date		
			PF	IORITY CLAII	M (35 U.S.C. 120)	
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	•
Keith M. Tackett Douglas H. Elliott	Registration No. 32,008 Registration No. 32,982

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Post Office Address:	Saratoga, CA 95070 SAME AS ABOVE U.S.A.	Country of Citizenship: USA		
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Inventor's signature:		Date:		
Residence:	10390 Stern Avenue			
Post Office Address:	Cupertino, CA 95014 SAME AS ABOVE U.S.A.	Country of Citizenship: TAIWAN		
Full name of seventh inventor:	~ // /	ADJAL		
Inventor's signature:	Parcagal	_ Date: 1_10.02		
Residence:	3655 Prineridge Avenu	ue #124		
Post Office Address:	Santa Clara, CA 9505 SAME AS ABOVE U.S.A.	Country of Citizenship: FRANCE		
Full name of eighth inventor:	JENNY C. LIN			
Inventor's signature:		Date:		
Residence: Post Office Address:	12725 Miller Avenue Saratoga, CA 95070 SAME AS ABOVE			
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Full name of second inventor: PAUL FREDERICK SMITH					
Inventor's signature:		Date:			
Residence:	225 E. Taylor Street #4 San Jose, CA 95112				
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·	U.U.A.	Country of Glazonomp.	
Full name of seventh inventor:	CHRISTOPHE MARCA	\DAL	
to a contract of the atoms		Data	
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riesidence.	Santa Clara, CA 9505		
Post Office Address:	SAME AS ABOVE		
	U.S.A.	Country of Citizenship: FRANCE	
Full name of eighth inventor:	IENNIV C I IN		
Full name of eighth inventor: JENNY C, LIN			
Inventor's signature:	A.Y	Date: 1/16/02 20532E1 Dorado (t.	
Residence:	12725 Miller Avenue	20532E1 Dorado Ct.	
	Saratoga, CA 95070	1.4.	
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